AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Currently Amended) A semiconductor device comprising:

a semiconductor layer;

a source region formed in the semiconductor layer;

a drain region formed in the semiconductor layer;

a channel region formed between the source region and the drain region in the semiconductor layer;

a gate insulating layer formed above the channel region; and

a gate electrode formed above the gate insulating layer, the gate electrode having a major axis and a minor axis;

wherein a boundary between the gate insulating layer and the channel region is a wave-like pattern of a gradual slope having crests and troughs alternately spaced apart along the major axis of the gate electrode.

2. (Currently Amended) A semiconductor device comprising:

a semiconductor layer;

a source region formed in the semiconductor layer;

a drain region formed in the semiconductor layer;

a channel region formed between the source region and the drain region in the semiconductor layer;

a gate insulating layer formed above the channel region; and

a gate electrode formed above the gate insulating layer, the gate electrode having a major axis and a minor axis;

wherein a boundary between the gate insulating layer and the channel region is a wave-like pattern without any corners, the wave-like pattern having crests and troughs alternately spaced apart along the major axis of the gate electrode.

3. (Original) The semiconductor device according to Claim 1, wherein a pitch between a top of the wave-like pattern and an adjacent bottom of the wave-like pattern in the boundary is less than or equal to 50 nm.

4. (Original) The semiconductor device according to Claim 2, wherein a pitch between a top of the wave-like pattern and an adjacent bottom of the wave-like pattern in the boundary is less than or equal to 50 nm.

5. (Original) The semiconductor device according to Claim 1, wherein a part of an upper surface of the source region is flat.

6. (Original) The semiconductor device according to Claim 2, wherein a part of an upper surface of the source region is flat.

7. (Original) The semiconductor device according to Claim 5, wherein a part of an upper surface of the drain region is flat.

8. (Original) The semiconductor device according to Claim 6, wherein a part of an upper surface of the drain region is flat.

9. (Original) The semiconductor device according to Claim 1, wherein the semiconductor layer is formed above a support substrate with an insulating layer therebetween.

10. (Original) The semiconductor device according to Claim 2, wherein the semiconductor layer is formed above a support substrate with an insulating layer therebetween.

11. (Cancelled)

12. (Currently Amended) A semiconductor device comprising:

a semiconductor layer;

a source region formed in the semiconductor layer;

a drain region formed in the semiconductor layer;

a channel region formed between the source region and the drain region in the semiconductor layer;

a gate insulating layer formed above the channel region; and

a gate electrode formed above the gate insulating layer, the gate electrode having a major axis and a minor axis;

wherein a boundary between the gate insulating layer and the channel region undulates and includes crests and troughs alternately spaced apart along the major axis of the gate electrode.

13. (Original) The semiconductor device according to Claim 12 wherein said boundary undulates in a sinusoidal pattern.

14. (Original) The semiconductor device according to Claim 12 wherein said boundary undulates in a curving pattern.